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(54) Nonlinear gray scale method and apparatus

(57) A display driver corrects the gray scale of a display (110) and increases the brightness dynamic range of the display (110) by producing a nonlinear gray scale for driving a display pixel (202) which is representative of the nonlinear response of the human eye. A nonlinear clock ($V_{NLCLOCK}$) is generated by counting to timeslot and segment data words representing the desired gray scale curve. The nonlinear clock ($V_{NLCLOCK}$) increments a pulse modulation counter (402) whose output is compared in a compare circuit (404) to the image's luminance data for generating a nonlinear pulse to activate the display pixel (202).

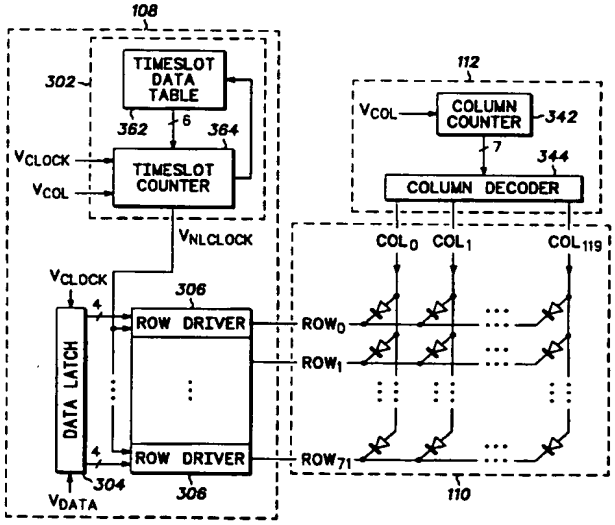

FIG. 3

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Description

Background of the Invention

The present invention relates in general to display devices and, more particularly, to gray scale correction of display devices.

Communications devices are frequently upgraded to provide greater functionality so that the devices receive and process increasing amounts of data. For example, pagers are reaching a level of complexity that requires a graphics user interface (GUI) to enable a user to control the operation of the pagers. A high resolution, emissive display such as an integrated light-emitting diode (LED) display provides a GUI for viewing graphics images which achieves high visibility at low power levels. Digital luminance data provides information needed for illuminating the LED display pixels to a desired level of brightness.

The LED pixels which comprise the LED display are characterized by a linear gray scale in which the LED pixels are illuminated in a finite series of equal luminance steps over the range of possible values of luminance data. Brightness is distinguished from luminance in that luminance is physically measurable whereas brightness is the subjective perception of luminance as viewed by the human eye. A problem with LED displays is that a linear luminance scale does not result in a linear brightness scale because the human eye has a nonlinear, logarithmic response to luminance. At low luminance levels, a small change in luminance is readily perceived as a change in brightness. However, at high luminance levels a comparable luminance change produces almost no perceptible change in brightness. The compression of brightness steps at higher luminance levels effectively reduces the brightness dynamic range of the display, giving most graphics images an inaccurate, washed-out appearance. The inaccuracy is especially noticeable on images which have been downloaded from a source such as the internet, because they typically have been preadjusted for displaying on a cathode ray tube, whose gray scale function is inherently nonlinear.

Hence, there is a need to correct digitally encoded images for viewing on a linear gray scale display device in order to portray the image more accurately to the human eye.

Brief Description of the Drawings

FIG. 1 is a block diagram of a wireless communications device;
FIG. 2 is a graph of luminance and brightness as a function of luminance data;
FIG. 3 is a schematic diagram of a display device coupled to row and column control circuits; and
FIG. 4 is a block diagram of a row driver circuit.

Detailed Description of the Drawings

FIG. 1 shows a block diagram of a wireless communications device 100, such as a pager or cellular telephone. Antenna 102, RF circuit 104 and demodulator 106 comprise a receiver circuit portion of wireless communication device 100. Antenna 102 receives a transmitted RF carrier signal which typically is modulated with digital signals such as control data for operating communications device 100 and video data representative of a downloaded image. The RF carrier signal is coupled to RF circuit 104 for tuning and amplification. The amplified RF carrier signal is received by demodulator 106 to recover a four bit, digital, video data stream V_{DATA} at a four conductor output bus 120, which is coupled to a data input of row control circuit 108. The width of output bus 120 can be varied as required by wireless communications device 100, including a single conductor which provides video data stream V_{DATA} in a serial mode. Video data stream V_{DATA} includes digital control information and a stream of four-bit luminance words for displaying a graphics image on display 110.

Display 110 is a display device which includes an array of LED devices organized into 72 rows and 120 columns. Display 110 has 72 rows coupled to nodes ROW_0 through ROW_{71} and to corresponding outputs of row control circuit 108. Display 110 has 120 columns coupled to nodes COL_0 through COL_{119} and to corresponding outputs of column control circuit 112. A LED pixel is illuminated when a column is selected and a row is activated.

Column control circuit 112 operates in a column scan mode in which one column of display 110 is selected by providing a column drive signal to display 110 on one of the nodes COL_0 through COL_{119}. Column control circuit 112 is repetitively clocked through the columns by a column select signal V_{COL}. The LED pixels in a selected column are activated in parallel by respective outputs of row control circuit 108. Luminance words of video data stream V_{DATA} are loaded into individual driver cells of row control circuit 108 by a system clock V_{CLOCK} typically operating at 1.25 megahertz. System clock V_{CLOCK} is a linear clock signal in that pulses are produced at equal time intervals. Row control circuit 108 controls the luminance of a selected LED pixel based on the value of the luminance word.

FIG. 2 shows a normalized graph of luminance and brightness as a function of the magnitude of video data stream V_{DATA} carrying luminance words for driving LED pixels in display 110. Luminance curve 21 shows the luminance pro-

duced by a LED pixel as a function of a luminance word. Luminance curve 21 thus represents the gray scale shading of the LED pixel as its luminance is varied over the range of the luminance word. Luminance curve 21 shows luminance to be linearly proportional to the luminance word such that equal increments in the magnitude of the luminance word produce equal increments in the luminance of the LED pixel.

Recall that the human eye perceives luminance logarithmically, i.e., nonlinearly, and that brightness is defined as perceived luminance. Brightness curve 22 shows the brightness of the LED pixel as it appears to a viewer. In effect, luminance curve 21 shows gray scale shading objectively in terms of emitted light and brightness curve 22 shows the gray scale shading subjectively in terms of a viewer's perception. Note that brightness curve 22 "flattens out" at higher levels, indicating a decreased "gain" of the human eye and an inability to distinguish luminance increments. When luminance of an image is displayed linearly as a function of luminance data, as in curve 21, much of the brightness range of the image is lost and the image seems washed-out.

It is preferable that an LED's brightness, rather than its luminance, be linear. In accordance with the present invention, a nonlinear correction represented by correction curve 23 is used to offset the nonlinearity of brightness curve 22 to produce a linear brightness function which is collinear with luminance curve 21. Correction curve 23 shows an ideal correction as a continuous function. However, in a digital system only discrete luminance magnitudes are produced whose resolution depends on the number of bits in a luminance word. In an embodiment of the present invention in which a luminance word comprises four bits, luminance of a LED pixel is produced in sixteen possible magnitudes corresponding to the sixteen possible values of a luminance word. The present invention implements four-bit, nonlinear gray scale shading by generating a discrete approximation of correction curve 23 to precorrect an activating signal prior to driving a LED pixel.

Referring to FIG. 3, a schematic diagram of display 110 driven by row control and column control circuits 108 and 112 are shown. Elements assigned the same reference number used in FIG. 1 provide a similar function. Display 110 includes an array of LED devices operating as display pixels organized into 72 rows and 120 columns. Each row is coupled to one of the nodes ROW_0 through ROW_{71}, and each column is coupled to one of the nodes COL_0 through COL_{119}. Each LED pixel has an anode and cathode uniquely connected to a column and a row for illuminating the LED pixel by driving the column and row with column and row drive signals. For example, LED 202 is illuminated by providing a column drive signal on node COL_0 and a row drive signal to node ROW_1.

To minimize flicker in display 110, a frame is refreshed at a 60.0 hertz rate, or every 16.7 milliseconds. Most LED displays are operated in a text mode in which the individual LEDs are either turned off or turned on to a fixed brightness level, rather than in a graphics mode where the brightness of each LED pixel is variable. In graphics mode, video data stream V_{DATA} comprises a sequence of four-bit luminance words which are recovered from video data stream V_{DATA} to control a brightness level of each LED pixel. In text mode, a single bit in video data stream V_{DATA} controls whether a LED pixel is turned off or turned on for a fixed period when the column is selected. Because more data is transferred in graphics mode than in text mode, more complex circuitry is needed. Graphics mode further requires circuits to convert the luminance word to a variable brightness level in the LED pixel.

The present invention produces a variable brightness level in a LED pixel by taking advantage of the integrating response of the human eye. During the 16.7 millisecond frame refresh period, each of the 120 columns is selected for a period of approximately 140 microseconds, or (16.7 milliseconds)/120. A row is active for a period of time determined by the value of the luminance word. The LED pixel is illuminated for the period when the column is selected and the row is active, such that the maximum luminance is produced when the row is active for 140 microseconds. For example, if the luminance word determines that ROW_1 is active for 70.0 microseconds while COL_0 is selected, then LED 202 is illuminated for 70.0 microseconds, thereby producing one-half of the maximum luminance. The human eye effectively integrates the luminance produced by LED 202 and perceives LED 202 as having a reduced brightness.

Column control circuit 112 includes a column counter 342 and a column decoder 344. Column counter 342 comprises a seven stage counter whose count is incremented one count on each pulse of column select signal V_{COL} received at a clock input. Column select signal V_{COL} has a period of 140 microseconds. At the maximum count of 119, column counter 342 wraps around to a zero count. A seven-bit output provides a binary column address which is decoded by column decoder 344 to sequentially assert a column select signal on nodes COL_0 through COL_{119} for selecting a column of display 110. After COL_{119} is selected, a column select signal is asserted on COL_0 and the cycle repeats.

Row control circuit 108 is shown including a data latch 304, a stack of 72 row drivers 306 and a nonlinear clock circuit 302. Data latch 304 is configured as a serial load, parallel out 72-stage shift register having a data capacity of four bits per stage. Video data stream V_{DATA} is clocked into a serial input of data latch 304 by system clock V_{CLOCK} to produce 72 luminance words at 72 four-bit outputs when data latch 304 is clocked by column select signal V_{COL}. The 72 four-bit outputs are coupled to data inputs of row drivers 306.

Row driver 306 is a pulse generator which produces a nonlinear, pulsewidth modulated pulse at one of the nodes ROW_0 through ROW_{71} having a pulsewidth determined by the value of the luminance word and nonlinear clock $V_{NL\text{-}CLOCK}$. The nonlinear pulse activates a LED pixel for a portion of the column select period to produce a luminance

whose gray scale shading is corrected by the nonlinear spacing of pulses of nonlinear clock $V_{NLCLOCK}$.

Nonlinear clock circuit 302 is a clock generator comprising a timeslot data table 362 and a timeslot counter 364. Nonlinear clock circuit 302 has a clock input for receiving system clock V_{CLOCK} running at 1.25 megahertz and an output for providing a free-running nonlinear clock $V_{NLCLOCK}$ to each row driver 306 in the stack of 72 row drivers. During the time when a column is selected, system clock V_{CLOCK} produces 174 pulses and nonlinear clock $V_{NLCLOCK}$ generates fifteen clock pulses for each of the values 1-15 of a four-bit luminance word. No pulse is generated if the luminance word equals zero. The fifteen pulses from $V_{NLCLOCK}$ are nonlinearly spaced to provide brightness correction determined by entries in timeslot data table 362.

Timeslot data table 362 comprises a plurality of memory locations for storing timeslot data words representing a number of pulses of system clock V_{CLOCK} over one period of column select clock V_{COL}. Following is a list of timeslot data words stored in timeslot data table 362 as well as the incremental spacing between successive pulses of nonlinear clock $V_{NLCLOCK}$ in an embodiment of nonlinear clock circuit 302 to demonstrate the nonlinearity of $V_{NLCLOCK}$ as shown in Table 1 below.

TABLE 1

$V_{NLCLOCK}$	# of V_{CLOCK} Pulses	Incremental change
15	174	25
14	149	22
13	127	19
12	108	17
11	91	15
10	76	13
9	63	11
8	52	10
7	42	9
6	33	8
5	25	7
4	18	5
3	13	5
2	8	4
1	4	4
0	0	

It should be apparent that other timeslot data words can be used to produce a clock whose pulses have a different relationship to each other for providing a different correction to a display.

Timeslot counter 364 is a parallel load, free-running down counter which is clocked by system clock V_{CLOCK}. Timeslot counter 364 has a load input for receiving a load pulse from column select signal V_{COL} when a new column is selected. Column select signal V_{COL} loads a timeslot data word into timeslot counter 364. Timeslot counter 364 is decremented by system clock V_{CLOCK} and, when a zero count is reached, a pulse of nonlinear clock signal $V_{NLCLOCK}$ is produced at the output of timeslot counter 364 and the next timeslot data word is loaded. The cycle repeats with a pulse of nonlinear clock $V_{NLCLOCK}$ being generated after system clock V_{CLOCK} counts the timeslot data word to decrement timeslot counter to zero. For greater flexibility and circuit economy, an alternative embodiment stores the number of pulses between successive pulses of $V_{NLCLOCK}$ in a timeslot data table and a separate segment data table stores the number of pulses of $V_{NLCLOCK}$ which are equally spaced. A parallel load, free-running segment counter can be decremented by the output of the timeslot counter.

FIG. 4 shows further detail of row driver 306 driving node ROW_0, including a pulse modulation counter 402, a compare circuit 404 and a R-S flip-flop 406. Pulse modulation counter 402 is a free-running up counter which counts from 0-15 in response to nonlinear clock $V_{NLCLOCK}$. Pulse modulation counter 402 produces a four-bit binary count at a four-bit output which is coupled to a first input of compare circuit 404. A second input of compare circuit 404 receives a lumi-

nance word from data latch 304.

When the value of the luminance word is zero, the output of compare circuit 404 holds flip-flop 406 in a reset state and prevents a nonlinear pulse from being generated. When the value of the luminance word is 1-15, column select signal V_{COL} resets pulse modulation counter 402 to a count of zero and sets flip-flop 406 to begin a nonlinear pulse at node ROW_0. The nonlinear pulse is terminated when the binary count of pulse modulation counter 402 reaches the value of the luminance word and compare circuit 404 resets flip-flop 406. In an alternative embodiment, pulse modulation counter 402 is configured as a parallel-loaded down counter such that the luminance word is loaded into pulse modulation counter 402, which decrements to zero to reset flip-flop 406 and terminate the nonlinear pulse. The width of the nonlinear pulse in terms of clock cycles of system clock V_{CLOCK} corresponds to the nonlinear pulse spacing of nonlinear clock $V_{NLCLOCK}$. The unequal increments of the nonlinear pulses provides the desired gray scale correction to improve the appearance of an image displayed on display 110.

By now it should be appreciated that a method and circuit has been shown for correcting the luminance of a linear gray scale display device to produce a linear brightness scale representative of the nonlinear response of the human eye. A nonlinear clock signal is generated by counting timeslot and segment data words corresponding to a piecewise linear approximation of the desired correction curve. The nonlinear clock increments a counter whose output is compared to the image's luminance data for a corresponding LED pixel, which generates a nonlinear pulse for illuminating the LED pixel.

While specific embodiments of the present invention have been shown and described, further modifications and improvements will occur to those skilled in the art. It is understood that the invention is not limited to the particular forms shown and it is intended for the appended claims to cover all modifications which do not depart from the spirit and scope of this invention. For example, the embodiment described herein provides correction circuitry for driving a display having 72 rows and 120 columns. One having ordinary skill in the relevant art could modify the circuits to adapt the present invention for driving a display with a different number of rows or columns or could provide a different correction curve than what is described herein.

Claims

1. A display driver, comprising:

   a clock generator (302) having an output for providing a non-linear clock signal ($V_{NLCLOCK}$); and
   a pulse generator (306) having a clock input responsive to the nonlinear clock signal and an output (ROW_0) for providing a nonlinear pulse for driving a display pixel.

2. The display driver of claim 1, wherein the clock generator includes:

   a timeslot counter (364) for counting to a timeslot word representative of a gray scale step to produce the nonlinear clock signal at an output.

3. The display driver of claim 2, wherein the clock generator further includes a timeslot data table (362) for storing the timeslot word for loading into the timeslot counter.

4. The display driver of claim 1, wherein the pulse generator includes a pulse modulation counter (402) having a clock input responsive to the nonlinear clock signal and an output coupled to the output of the pulse generator.

5. The display driver of claim 4, wherein the pulse generator further includes a compare circuit (404) having a first input coupled for receiving a luminance signal, a second input coupled to the output of the pulse modulation counter, and an output coupled for driving the display pixel.

6. The display driver of claim 5, wherein the pulse generator further includes a flip-flop (406) having a first input responsive to an activation signal (V_{COL}), a second input coupled to the output of the compare circuit and an output for providing the nonlinear pulse.

7. A method for producing a desired brightness level in a display, comprising a step of driving a display pixel with a pulsewidth modulated signal.

8. The method of claim 7, further comprising the steps of:

   generating a non-linear clock signal ($V_{NLCLOCK}$); and

counting a luminance word with the non-linear clock signal to produce the pulsewidth modulated signal.

9. The method of claim 8, wherein the step of counting includes comparing a count signal with the luminance word.

10. A wireless communications device (100), comprising:

a radio frequency (RF) circuit (104, 106) having an input for receiving a RF signal modulated with a video signal (V_{DATA}), wherein the RF circuit includes a demodulator (106) for recovering the video signal (V_{DATA}) at an output;
a display device (110) having a display pixel; and
a display driver which includes,

(a) a clock generator (302) having an output for providing a non-linear clock signal ($V_{NLCLOCK}$); and
(b) a pulse generator (306) having a clock input responsive to the nonlinear clock signal ($V_{NLCLOCK}$), a data input responsive to the video signal and an output (ROW_0) for providing a nonlinear pulse for driving the display pixel.

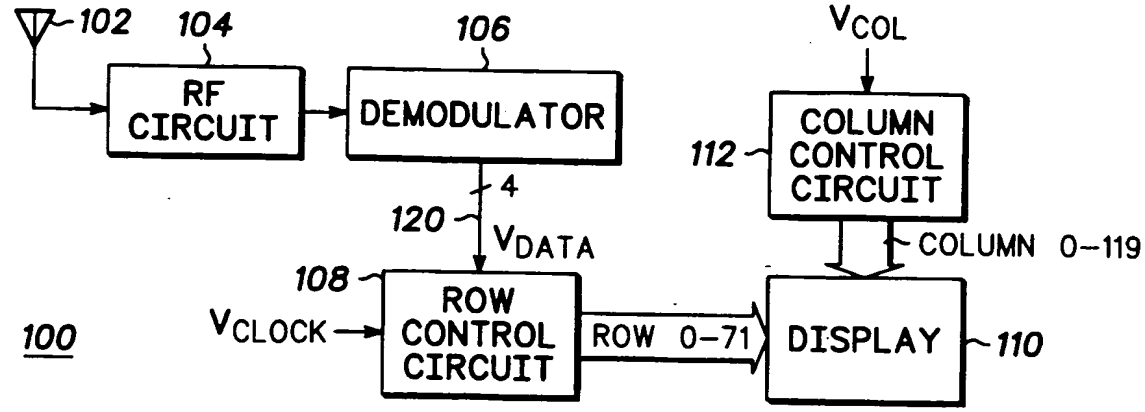

FIG. 1

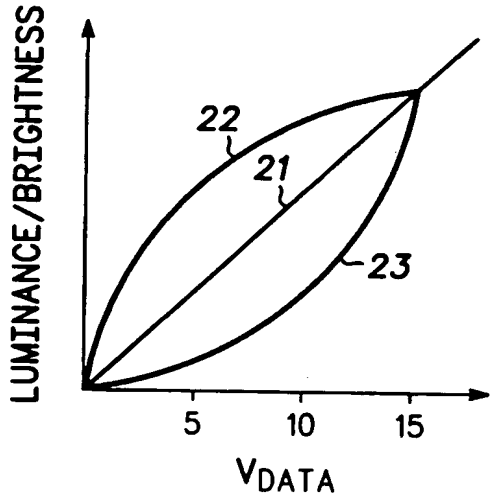

FIG. 2

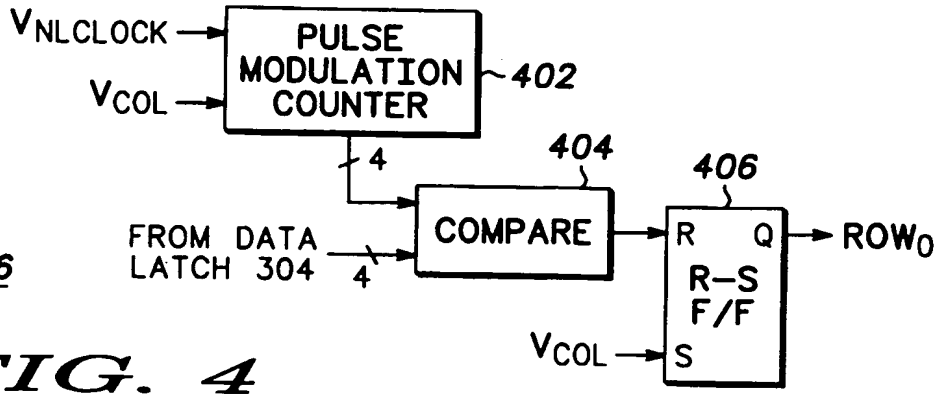

FIG. 4

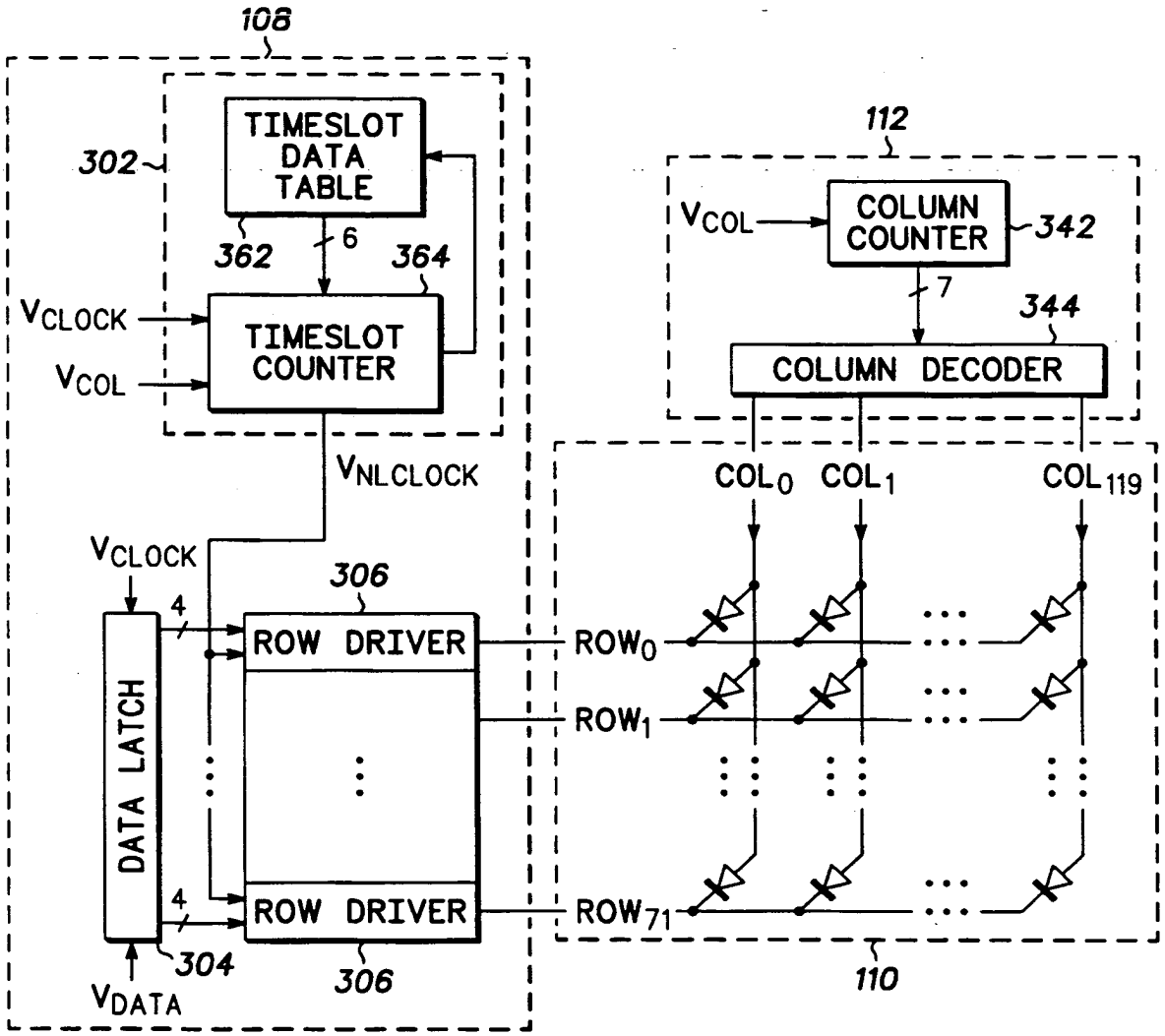

FIG. 3

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EUROPEAN SEARCH REPORT

Application Number
EP 97 11 6848

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	GB 2 204 174 A (SEIKO INSTRUMENTS INC) 2 November 1988	1,2,4-9	G09G3/32
A	* abstract; figures 7-11 * * page 2, line 13 - page 3, line 5 * * page 9, line 16 - page 13, line 25 *	3,10	
A	US 4 255 793 A (NAKAMURA) 10 March 1981 * abstract; figure 9 * * column 9, line 23 - column 10, line 33 *	3	
A	WO 90 03023 A (CHIPS AND TECHNOLOGIES, INC) 22 March 1990 * abstract; figures 3,6,7 * * page 12, line 1 - page 13, line 5 *	7	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	6 February 1998	Van Roost, L

CATEGORY OF CITED DOCUMENTS

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